UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/614,341	07/02/2003	Matti Floman	944-001.112	7863

4955 7590 05/16/2005

WARE FRESSOLA VAN DER SLUYS &
ADOLPHSON, LLP
BRADFORD GREEN BUILDING 5
755 MAIN STREET, P O BOX 224
MONROE, CT 06468

EXAMINER	
TABONE JR, JOHN J	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 05/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/614,341	FLOMAN ET AL.	
	Examiner	Art Unit	
	John J. Tabone, Jr.	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

FINAL DETAILED ACTION

1. Claims 1-33 are pending in this application and have been examine.

2. The Applicant has not overcome the claim objection for misnumbered claim 32 (second appearance). The Applicant must make the correction by renumbering claim 32 (second appearance) to claim 33 in a subsequent amendment.

Response to Arguments

3. Applicant's arguments filed 12/06/2004 have been fully considered but they are not persuasive.

As per arguments for claims 1 and 18:

The Applicant states "Coyle does not disclose determining the bus width of a device that is connected to a host device". The Examiner would like to point out that the above-cited limitation does not appear in claims 1, 18 or any of the other independent claims 12 and 24. Therefore, in response to Applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., determining the bus width of a device that is connected to a host device) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

The Applicant states "Cedar does not disclose or even suggest sending through the data bus a certain bit pattern to a memory card and receiving through the same data bus a return bit pattern so that the data bus width can be determined based on the relationship between the sent bit pattern and the returned bit pattern." The Examiner would like to point out that the above-cited limitation does not appear in claims 1, 18 or any of the other independent claims 12 and 24. Therefore, in response to Applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., sending through the data bus a certain bit pattern to a memory card and receiving through the same data bus a return bit pattern so that the data bus width can be determined based on the relationship between the sent bit pattern and the returned bit pattern) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

It is the Examiner's conclusion that independent claims 1, 12, 18 and 24 are not patentably distinct or non-obvious over the prior arts of record namely, Kim et al. (US-6108802) in view of Martens (US-5751727). Therefore, the rejection is maintained. Based on their dependency on claims 1, 12, 18 and 24, claims 2-11, 13-17, 19-23 and 25-32 (second appearance), respectively, stand rejected.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cedar et al. (WO-02/15020), hereinafter, Cedar, in view of Coyle et al. (US-6473871), hereinafter Coyle.

Claims 1 and 18:

Cedar teaches a host 51" (first electronic module) connected to multiple memory card sockets 104, 106, and 108 over more than one data line (data bus). Cedar teaches sockets 104, 106, and 108 contain Security Digital (SD) memory cards (second electronic module) which have an increased number of data contacts (data bus). Cedar also teaches the host determines the data bus width of the SD card by reading (host's read command is first bit pattern) the SD Card Configuration Register (SCR) (SCR data is second bit pattern). Cedar further teaches that the data identifying the data bus width is read from the SCR is stored by the host in a table form (receiving in the first electronic module the second bit pattern from the second electronic module). (Fig. 8, page 15, lines 28-32, page 16, lines 1-3, 30-32). Cedar does not explicitly teach "the second bit pattern having a predetermined relationship with the first bit pattern". However, Cedar does teach the host controller 51' generates streams of data which the host 51" outputs in parallel and is received by the data register 35' within the SD Card. Cedar also

teaches when the host 51" also reads data from the SD card the data is loaded in parallel into register 35' and sent over the data lines. (Figure 2, page 14, lines 14-28, page 15, lines 12-14). Coyle teaches an electronic system 100 which can be a communication device such as a cellular phone having first and second devices 102, 104 (first and second electronic modules) interconnected for communication by a bus 106. (Col. 6, lines 47-60). Coyle also teaches that bus testing logic 120, which can be implemented in software, for testing the bus 106 by injecting a predetermined sequence of voltage levels, high or low (1's and 0's), so that they can be analyzed after traversing the bus. Coyle illustrates in FIG. 2B, a loopback testing methodology 220, in which (a) a driver end 222, e.g., at first device 102 (first electronic module) of FIG. 1, sends a predetermined bus testing voltage pattern (1's and 0's) (first bit pattern) over the bus 205 to a receiver end 224, e.g., at second device 104 (second electronic module) of FIG. 1, and (b) the receiver end 224 stores the received pattern and forwards it back to the driver end 222 as a reverse pattern (second bit pattern). (Col. 7, lines 8,9, 42-53). It would have been obvious to one of ordinary skill in the art to modify Cedar's host 51" (first electronic modules), which includes host controller 51', to execute Coyle's bus testing logic 120 to send predetermined sequence of voltage levels, high or low (1's and 0's), to the (SD) memory cards (second electronic module) contained in sockets 104, 106, and 108 for test a bus. It also would have been obvious to one of ordinary skill in the art to modify Cedar's (SD) memory cards (second electronic module) contained in sockets 104, 106, and 108 to include the processor in Coyle's bus testing logic 120 to enable Cedar's (SD) memory cards (second electronic module) to return the reverse

pattern (second bit pattern) over the data lines once the data is loaded in parallel into register 35'. The artisan would have been motivated to do so because it would give Cedar the ability to dynamically select the width of the data bus between the host 51" and the SD memory card(s). The artisan also would have been motivated to do so because it would maximize the data rate between the host and the SD memory card(s).

Claim 12:

Cedar teaches a host 51" (first electronic module) connected to multiple memory card sockets 104, 106, and 108 over more than one data line (data bus). Cedar teaches sockets 104, 106, and 108 contain Security Digital (SD) memory cards (second electronic module) which have an increased number of data contacts (data bus). Cedar also teaches the host determines the data bus width of the SD card by reading (host's read command is first bit pattern) the SD Card Configuration Register (SCR) (SCR data is second bit pattern). Cedar further teaches that the data identifying the data bus width is read from the SCR is stored by the host in a table form (receiving in the first electronic module the second bit pattern from the second electronic module). (Fig. 8, page 15, lines 28-32, page 16, lines 1-3, 30-32). Cedar does not explicitly teach "the second bit pattern having a predetermined relationship with the first bit pattern". However, Cedar does teach the host controller 51' generates streams of data which the host 51" outputs in parallel and is received by the data register 35' within the SD Card. Cedar also teaches when the host 51" also reads data from the SD card the data is loaded in parallel into register 35' and sent over the data lines. (Figure 2, page 14, lines 14-28, page 15, lines 12-14). Coyle teaches an electronic system 100 which can be a

communication device such as a cellular phone having first and second devices 102, 104 (first and second electronic modules) interconnected for communication by a bus 106. (Col. 6, lines 47-60). Coyle also teaches that bus testing logic 120, which can be implemented in software, (a software program for use in a first electronic module) for testing the bus 106 by injecting a predetermined sequence of voltage levels, high or low (1's and 0's), so that they can be analyzed after traversing the bus. Coyle illustrates in FIG. 2B, a loopback testing methodology 220, in which (a) a driver end 222, e.g., at first device 102 (first electronic module) of FIG. 1, sends a predetermined bus testing voltage pattern (1's and 0's) (first bit pattern) over the bus 205 to a receiver end 224, e.g., at second device 104 (second electronic module) of FIG. 1, and (b) the receiver end 224 stores the received pattern and forwards it back to the driver end 222 as a reverse pattern (second bit pattern). (Col. 7, lines 8,9, 42-53). Coyle teaches a way to analyze the results would be to compare (code for comparing) the source pattern 340 (first bit pattern) with the received pattern 350 (second bit pattern) on a cell-by-cell or bit-by-bit basis. (Col. 10, lines 34-37). It would have been obvious to one of ordinary skill in the art to modify Cedar's host 51" (first electronic modules), which includes host controller 51', to execute Coyle's bus testing logic 120 to send predetermined sequence of voltage levels, high or low (1's and 0's), to the (SD) memory cards (second electronic module) contained in sockets 104, 106, and 108 for test a bus. It also would have been obvious to one of ordinary skill in the art to modify Cedar's (SD) memory cards (second electronic module) contained in sockets 104, 106, and 108 to include the processor in Coyle's bus testing logic 120 to enable Cedar's (SD) memory cards (second electronic

module) to return the reverse pattern (second bit pattern) over the data lines once the data is loaded in parallel into register 35'. The artisan would have been motivated to do so because it would give Cedar the ability to dynamically select the width of the data bus between the host 51" and the SD memory card(s). The artisan also would have been motivated to do so because it would maximize the data rate between the host and the SD memory card(s).

Claims 24 and 25:

Cedar teaches a host 51" (data processing unit) connected to multiple memory card sockets 104, 106, and 108 over more than one data line (data bus). Cedar teaches sockets 104, 106, and 108 contain Security Digital (SD) memory cards (memory unit) which have an increased number of data contacts (data bus). Cedar also teaches the host determines the data bus width of the SD card by reading (host's read command is first bit pattern) the SD Card Configuration Register (SCR) (SCR data is second bit pattern). Cedar further teaches that the data identifying the data bus width is read from the SCR is stored by the host in a table form (receiving in the first electronic module the second bit pattern from the second electronic module). (Fig. 8, page 15, lines 28-32, page 16, lines 1-3, 30-32). Cedar does not explicitly teach "the second bit pattern having a predetermined relationship with the first bit pattern". However, Cedar does teach the host controller 51' generates streams of data which the host 51" outputs in parallel and is received by the data register 35' within the SD Card. Cedar also teaches when the host 51" also reads data from the SD card the data is loaded in parallel into register 35' and sent over the data lines. (Figure 2, page 14, lines 14-28, page 15, lines

12-14). Coyle teaches an electronic system 100 which can be a communication device such as a cellular phone having first and second devices 102, 104 (first and second electronic modules) interconnected for communication by a bus 106. (Col. 6, lines 47-60). Coyle also teaches that bus testing logic 120, which can be implemented in software, (a software program for use in a first electronic module) for testing the bus 106 by injecting a predetermined sequence of voltage levels, high or low (1's and 0's), so that they can be analyzed after traversing the bus. Coyle illustrates in FIG. 2B, a loopback testing methodology 220, in which (a) a driver end 222, e.g., at first device 102 (data processing unit) of FIG. 1, sends a predetermined bus testing voltage pattern (1's and 0's) (first bit pattern) over the bus 205 to a receiver end 224, e.g., at second device 104 (memory unit) of FIG. 1, and (b) the receiver end 224 stores the received pattern and forwards it back to the driver end 222 as a reverse pattern (second bit pattern). (Col. 7, lines 8,9, 42-53). Coyle teaches a way to analyze the results would be to compare (code for comparing, Claim 25) the source pattern 340 (first bit pattern) with the received pattern 350 (second bit pattern) on a cell-by-cell or bit-by-bit basis. (Col. 10, lines 34-37). It would have been obvious to one of ordinary skill in the art to modify Cedar's host 51" (data processing unit), which includes host controller 51', to execute Coyle's bus testing logic 120 to send predetermined sequence of voltage levels, high or low (1's and 0's), to the (SD) memory cards (memory unit) contained in sockets 104, 106, and 108 for test a bus. It also would have been obvious to one of ordinary skill in the art to modify Cedar's (SD) memory cards (memory unit) contained in sockets 104, 106, and 108 to include the processor in Coyle's bus testing logic 120 to enable Cedar's

(SD) memory cards (memory unit) to return the reverse pattern (second bit pattern) over the data lines once the data is loaded in parallel into register 35'. The artisan would have been motivated to do so because it would give Cedar the ability to dynamically select the width of the data bus between the host 51" and the SD memory card(s). The artisan also would have been motivated to do so because it would maximize the data rate between the host and the SD memory card(s).

Claims 2 and 19:

The motivation to combine Cedar's host 51" and SD memory card(s) to include Coyle's bus testing logic 120 is rejected as per claim 1. Coyle teaches a way to analyze the results would be to compare the source pattern 340 (first bit pattern) with the received pattern 350 (second bit pattern) on a cell-by-cell or bit-by-bit basis. (Col. 10, lines 34-37).

Claims 3, 20, and 31:

The motivation to combine Cedar's host 51" and SD memory card(s) to include Coyle's bus testing logic 120 is rejected as per claim 1. Coyle illustrates in FIG. 2B, a loopback testing methodology 220, in which (a) a driver end 222, e.g., at first device 102 (first electronic module) of FIG. 1, sends a predetermined bus testing voltage pattern (1's and 0's) (first bit pattern) over the bus 205 to a receiver end 224, e.g., at second device 104 (second electronic module) of FIG. 1, and (b) the receiver end 224 stores the received pattern and forwards it back to the driver end 222 as a reverse pattern (second bit pattern).

Claims 4, 14, and 32:

The motivation to combine Cedar's host 51" and SD memory card(s) to include Coyle's bus testing logic 120 is rejected as per claim 1. Coyle illustrates in FIG. 2B, a loopback testing methodology 220, in which (a) a driver end 222, e.g., at first device 102 (first electronic module) of FIG. 1, sends a predetermined bus testing voltage pattern (1's and 0's) (first bit pattern) over the bus 205 to a receiver end 224, e.g., at second device 104 (second electronic module) of FIG. 1, and (b) the receiver end 224 stores the received pattern and forwards it back to the driver end 222 as a reverse pattern (second bit pattern is the compliment).

Claims 5 and 16:

Cedar teaches can be designed to operate with a lesser number of data lines. (Page 16, lines 5,6).

Claims 6 and 17:

The motivation to combine Cedar's host 51" and SD memory card(s) to include Coyle's bus testing logic 120 is rejected as per claim 1. Coyle illustrates in FIG. 2B, a loopback testing methodology 220, in which (a) a driver end 222, e.g., at first device 102 (first electronic module) of FIG. 1, sends a predetermined bus testing voltage pattern (1's and 0's) (first bit pattern) over the bus 205 to a receiver end 224, e.g., at second device 104 (second electronic module) of FIG. 1, and (b) the receiver end 224 stores the received pattern and forwards it back to the driver end 222 as a reverse pattern (second bit pattern). (Col. 7, lines 8,9, 42-53). It would have been obvious to one of ordinary skill in the art that Coyle's predetermined bus testing voltage pattern (1's and

0's) would include subsequent data patterns that would be a compliment of the previously sent patterns. The artisan would have been motivated to do so because sending the compliment bit pattern would further test the bus pins for faults.

Claim 7:

This claim is rejected as per claim 2.

Claim 8:

Cedar teaches a host 51" (first electronic module) connected to multiple memory card sockets 104, 106, and 108 over more than one data line (data bus). Cedar teaches sockets 104, 106, and 108 contain Security Digital (SD) memory cards (second electronic module comprises a memory card) which have an increased number of data contacts (data bus).

Claims 9 and 22:

Cedar teaches a method to adapt the host (first electronic module) to cards with different data bus widths, to do so dynamically as cards are substituted or added, and even communicate with each of a mixture of cards having different bus widths (number data pins is equal) by using the maximum number of data lines the individual cards. (Page 16, lines 15-18).

Claims 10 and 21:

Cedar teaches a method to adapt the host (first electronic module) to cards with different data bus widths, to do so dynamically as cards are substituted or added, and even communicate with each of a mixture of cards having different bus widths (number data pins is smaller) by using the maximum number of data lines the individual cards.

(Page 16, lines 15-18).

Claims 11 and 23:

Cedar teaches a method to adapt the host (first electronic module) to cards with different data bus widths, to do so dynamically as cards are substituted or added, and even communicate with each of a mixture of cards having different bus widths (number data pins is greater) by using the maximum number of data lines the individual cards. (Page 16, lines 15-18).

Claim 13:

Cedar teaches the host determines the data bus width of the SD card by reading (code for determining a usable bus width) the SD Card Configuration Register (SCR). (Page 16, lines 30-32).

Claim 15:

Cedar teaches the host determines the data bus width of the SD card by reading (code for generating the first bit pattern) the SD Card Configuration Register (SCR) (SCR data is second bit pattern). (Page 16, lines 30-32).

Claim 26:

Cedar teaches the host determines the data bus width of the SD card by reading (code for determining a usable data width) the SD Card Configuration Register (SCR) (SCR data is second bit pattern). (Page 16, lines 30-32).

Claim 27:

Cedar teaches host 51" determines the data bus width of the SD card by reading (code for determining a usable data width) the SD Card Configuration Register (SCR)

upon power-up. (Page 15, lines 31, 32, page 16, lines 1-3).

Claim 28:

Cedar teaches the disclosed memory card(s) contain non-volatile semiconductor flash EPROM systems have become popular for storing multiple megabytes of data from personal computers, notebook computers, personal electronic assistants, cellular phones (mobile phone), cameras and other electronic devices requiring removable data storage. (Page 1, lines 14-17).

Claim 29:

This claim is rejected per claim 28 above.

Claim 30:

This claim is rejected as per claims 1 and 18 above.

Claim 33:

This claim is rejected per claim 6 above.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J. Tabone, Jr. whose telephone number is (571) 272-3827. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John J. Tabone, Jr.
Examiner
Art Unit 2133

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CE